REMARKS

Claims 1-6 are currently pending in the application.

Priority

Applicants request acknowledgment of the receipt of the certified copy of the priority document (JP 2000-298525, filing date September 29, 2000) submitted on May 25, 2004. A copy of the mailroom date-stamped receipt is enclosed as evidence that the document was submitted.

Attachment: Filing Receipt of May 25, 2004

Oath/Declaration

The Examiner informed Applicant's attorney by telephone on May 25, 2004, that an executed Declaration had not been received in this case. The executed Declaration was originally filed on November 27, 2001, in response to the Notice to File Missing Parts mailed on September 28, 2001. A copy of the mailroom date-stamped receipt is attached showing that the executed Declaration was filed and that the surcharge of $130 was paid on November 27, 2001, so it is believed that no additional fee is due.

Additionally, on May 25, 2004, in response to the telephone call from the Examiner, Applicant filed a copy of the executed Declaration for this case. This was filed on May 25, 2004, as evidenced by the attached copy of the mailroom date-stamped receipt. It is believed that the Declaration had not yet been matched with the file at the time the Examiner prepared the Office Action of June 2, 2004, but that the Declaration has by now been matched with the file. Accordingly, it is believed that no further action on the part of the Applicant is required. Should the second copy of the Declaration have not been matched with the application file by the time this Reply is received, the Examiner is urged to contact Applicant's undersigned attorney by telephone so that another copy of the Declaration can be provided.

Attachments: Filing receipt of November 27, 2001, and
Filing Receipt of May 25, 2004.

Drawings

Four sheets of formal drawings are attached to this Reply, containing FIGS. 1, 4, 5 and 6. As set forth in detail above, in the section entitled "Amendments to the Drawings", the drawings filed with this Reply are believed to fully

address each and every objection raised in the Office Action. Accordingly, withdrawal of the objection to the drawings is requested.

35 U.S.C. §103

Claims 1 and 2 stand rejected under 35 U.S.C. § 103 as being unpatentable over Ramamurthy et al. (US 5,787,114) in view of Sasaki et al. (US 4,833,395) and Funatsu (US 4,225,958). In addition, claims 3-5 stand rejected under 35 U.S.C. § 103 as being unpatentable over Ramamurthy, Sasaki, and Funatsu, and further in view of Ushikoshi (US 4,545,686). Furthermore, claim 6 stands rejected under 35 U.S.C. § 103 as being unpatentable over Ramamurthy, Sasaki, and Funatsu, and further in view of Katayama (US 5,353,434).

The combination of the structural elements of the invention set forth in claim 1 includes an operation judging circuit. (See, e.g., item 16 in FIG. 3, and the specification beginning at Page 14, Line 12.) As set forth in claim 1, the operation judging circuit includes a plurality of second circuits (see, e.g., flip-flop circuits 301-331 in FIG. 3) each capable of holding a value of one pulse in its associated one of the pulse sequences of the response parallel signals received from the receiving circuit (see, e.g., item 15 in

FIG. 1); a plurality of third circuits (see, e.g., exclusive OR circuits 341-356 in FIG. 3) for generating expected values for pulses of pulse sequences in the response parallel signals received from the receiving circuit after the pulses whose signal values have been held, based on signal values held in the second circuits; and a plurality of fourth circuits (see, e.g., exclusive NOR circuits 361-376 in FIG. 3) for comparing values of pulses of the pulse sequences in the response parallel signals received from said receiving circuit with the expected values generated by said third circuits. The third circuits generate the expected values in a parallel manner and the fourth circuits compare the expected values with the outputs of the receiving circuit in a parallel manner so as to make a judgment for the quality of the semiconductor circuit based on the comparison result.

Accordingly, the operation judging circuit enables the expected values to be obtained on the basis of the output signals of the receiving circuit. Therefore, it is not necessary to take the test pattern signal generated by the test signal generating circuit into the operation judging circuit as the expected values. As a result, a signal transfer path for supplying the test pattern signal from the test signal generating circuit to the operation judging

circuit becomes unnecessary. In addition, in the signal comparison in the operation judging circuit, it is not necessary to synchronize the signal with respect to the test signal generating circuit. (See, e.g., Page 29, Lines 4-16 of the specification.) Because of this, a synchronizing circuit for synchronization between the test signal and the output signal of the receiving circuit is not required in the present invention.

The cited reference to Ramamurthy et al. discloses a loop back test system for an integrated circuit device. The test system comprises a transmitter that includes a serializer, an output buffer and a clock generator; a receiver that includes an input buffer, a deserializer, a clock generator and a data alignment unit; a loopback path connecting the transmitter and the receiver; and a built-in self test (BIST) unit. Ramamurthy does not disclose the operation of the BIST unit and does not disclose an operation judging circuit as set forth in claim 1. Accordingly, the structural combination defined in claim 1, including the operation judging circuit, is not taught from Ramamurthy et al.

Similarly, the cited reference to Sasaki et al. shows a test signal generating circuit 12, a test circuit 15, and a logic circuit 14 to be tested. The test signal obtained from

the test circuit 15 is passed through an ON transmission gate TG6 and a buffer amplifier 29 of an output buffer 16, and is supplied to an external output terminal 30. (See, Column 4, Lines 11-14 of Sasaki.) A signal pattern of the signal obtained from the external output terminal 30 is tested on an LSI tester that is not shown (see Column 4, Lines 14-17). Thus, Sasaki also does not include an operation judging circuit and does not teach the structural combination defined by claim 1 of the present application.

The cited reference to Funatsu shows an LSI comprising a logic circuit, signal holding circuits, and an electric circuit. Funatsu is silent as to how to judge whether the LSI passes or fails testing. Therefore, Funatsu does not teach an operating judging circuit or the combined elements of the invention as defined in claim 1.

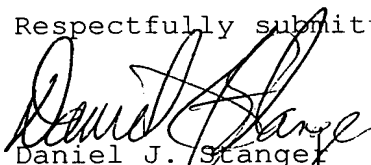
Accordingly, Applicants respectfully assert that claim 1 is allowable over Ramamurthy, Sasaki, Funatsu, and the other art of record, taken either singly, or in combination. The art of record does not show or suggest a semiconductor integrated circuit formed on a single semiconductor chip that includes the operation judging circuit of the invention combined with the other structural elements defined in claim 1. Furthermore, dependent claims 2-6 include additional

elements of the claimed combination, and are also asserted to be allowable at least because they depend from allowable base claim 1.

Conclusion

In view of the foregoing amendments and remarks, Applicants submit that the above-identified application is now in condition for allowance. Accordingly, reconsideration and reexamination are respectfully requested.

Respectfully submitted,



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Date: September 2, 2004

ASA-1026

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In re Patent Application of

K. WATANABE et al

Serial No. 09/939,589 Group Art Unit: 2133

Filed: August 28, 2001 Examiner: D. Gandhi

For: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING A SELF-TESTING FUNCTION

Papers Filed Herewith:

TRANSMITTAL OF CERTIFIED PRIORITY DOCUMENT; and
Certified copy of JP 2000-298525.

Receipt is hereby acknowledged of the papers filed, as identified in connection with the above-identified patent application.

COMMISSIONER OF PATENTS AND TRADEMARKS

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Filed: August 28, 2001 Examiner: D. Gandhi

For: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING A SELF-TESTING FUNCTION

Papers Filed Herewith:

SUBMISSION OF COPY OF DECLARATION AND OTHER DOCUMENTS;
Copy of executed Declaration; and
Copy of PTO date-stamped receipt.

Receipt is hereby acknowledged of the papers filed, as identified in connection with the above-identified patent application.

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Serial No. 09/939,589

Filed: August 28, 2001

For: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING A SELF-TESTING FUNCTION

Papers Filed Herewith:

TRANSMITTAL OF LATE DECLARATION;
Executed Declaration and Power of Attorney;
Copy of NOTICE; and
Check No. 4983 in the amount of $130.00 in payment of Surcharge for Late Declaration.

Receipt is hereby acknowledged of the papers filed, as identified in connection with the above-identified patent application.

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